IN THE CLAIMS

Please cancel Claim 1 without prejudice or disclaimer.

Claim 1 (cancelled)

Claim 2 (currently amended): In a PWM switching power output stage circuit, an over-current detection method comprising the steps of:

detecting a pulse width of a PWM signal;

detecting an over-current condition in the PWM circuit;

adaptively filtering a detected over-current condition relative to the pulse width; and

generating an over-current detection output,

~~A method according to claim 1~~ wherein the adaptively filtering step further comprises selecting a digital delay less than the pulse width of the PWM signal to ensure reliable detection.

Claim 3 (currently amended): In a PWM switching power output stage circuit, an over-current detection method comprising the steps of:

detecting a pulse width of a PWM signal;

detecting an over-current condition in the PWM circuit;

adaptively filtering a detected over-current condition relative to the pulse width; and

generating an over-current detection output,

~~A method according to claim 1~~ further comprising the step of providing a plurality of selectable digital delays for adaptively filtering the detected over-current condition.

Claim 4 (original): A method according to claim 2 further comprising the step of providing at least one selectable digital delay of less than one half of a pre-selected minimum pulse width of the PWM circuit.

Claim 5 (currently amended): In a PWM switching power output stage circuit, an over-current detection method comprising the steps of:

detecting a pulse width of a PWM signal;

detecting an over-current condition in the PWM circuit;

adaptively filtering a detected over-current condition relative to the pulse width; and

generating an over-current detection output,

~~A method according to claim 1~~ wherein the outputting step further comprises outputting a positive over-current detection result for an over-current detection signal having a duration equal to or greater than ~~the~~ a selected digital delay.

Claim 6 (currently amended): An over-current detection method for application in a PWM switching power output stage circuit, the over-current detection method comprising the steps of:

detecting ~~the~~ a pulse width of a PWM signal in the PWM circuit;

selecting a digital delay less than the pulse width of the PWM signal;

detecting an over-current condition in the PWM circuit and providing an over-current detection signal;

filtering the over-current detection signal by means of the digital delay; and

outputting an over-current detection result.

Claim 7 (original): A method according to claim 6 further comprising the step of providing a plurality of selectable digital delays.

Claim 8 (original): A method according to claim 6 further comprising the step of providing at least one selectable digital delay of less than one half of a pre-selected minimum pulse width of the PWM circuit.

Claim 9 (original): A method according to claim 6 wherein the filtering step further comprises the step of logically determining that the over-current detection signal and the selected digital delay are both true.

Claim 10 (original): A method according to claim 6 wherein the outputting step further comprises outputting a positive over-current detection result for an over-current detection signal having a duration equal to or greater than the selected digital delay.

Claim 11 (currently amended): An over-current detection method for PWM switching power stages, the over-current detection method comprising the steps of:

providing a plurality of selectable digital delays, at least one selectable digital delay having a duration less than one half of a pre-selected minimum pulse width of the PWM circuit;

detecting ~~the~~ a pulse width of a PWM signal in the PWM circuit;

selecting a digital delay less than the pulse width of the PWM signal;

detecting an over-current condition in the PWM power stage and providing an over-current detection signal;

filtering the over-current detection signal by means of logically determining whether the over-current detection signal and ~~the~~ a selected delayed OC detection signal are both true; and

outputting an over-current detection result for an over-current detection signal having a duration greater than the selected digital delay.

Claim 12 (currently amended): An over-current detection circuit for use in a PWM switching power stage, the over-current detection circuit comprising:

a plurality of selectable digital delay paths;

a pulse width detection circuit for detecting ~~the~~ a pulse width of a PWM signal in ~~the~~ a PWM system;

an over-current condition detector for detecting the presence of an over-current in the PWM system;

a filter for outputting an over-current detection result for an over-current detection signal having a duration equal to or greater than the selected digital delay.

Claim 13 (original): An over-current detection circuit according to claim 12 further comprising at least one selectable digital delay path having a duration less than one half of a pre-selected minimum pulse width of the PWM circuit.

Claim 14 (original): An over-current detection circuit according to claim 12 further comprising digital logic means for detecting the presence of an over-current detection signal having a duration greater than the selected digital delay.